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TECHNICAL PAPER

Designing for Successful Flash Memory Read and Verify Operations

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1.0 INTRODUCTION

This technical paper documents hardware and software techniques to eliminate read and verify problems caused by V_{CC} and GND transient voltage spikes. These transient voltage spikes can be encountered in any of the following environments:

- PROM Programmers
- On-Board Programming systems
- Embedded applications

As flash memory manufacturing processes improve, silicon geometries get smaller and device timing parameters get faster. These process improvements help reduce costs of the flash product.

A recent process improvement at Intel Corporation brought faster output slew rates to our flash memory components (see Figures 1 and 2). In properly designed applications, the faster output slew rates have no affect on system operation, but in marginally designed applications the faster slew rates triggered false read and verify errors. These false read and verify errors are random, meaning each time read and verify is performed the failing location is different. The errors occur from a combination of different factors described in this document.

The techniques discussed in this technical paper have been implemented successfully in various programmer and embedded system environments. These suggestions are intended to help reliably operate Intel Flash components in any system environment. Please remember that each environment is unique. Optimizations which reduce noise transitions in one instance may not apply to every design.

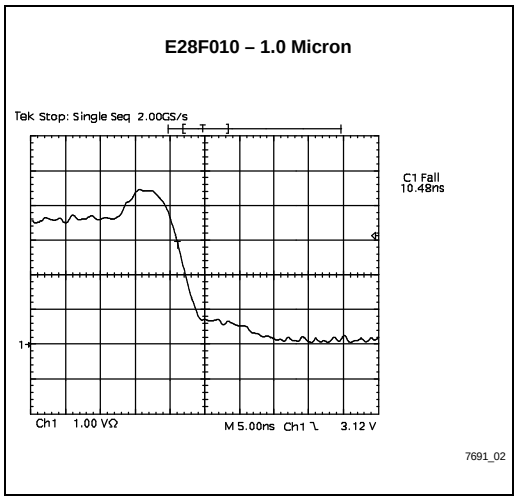

Figure 1. Older Process 1.0 Micron Intel Flash Memory Devices Have Slow Output Slew Rates, 10.48 ns, in This Case

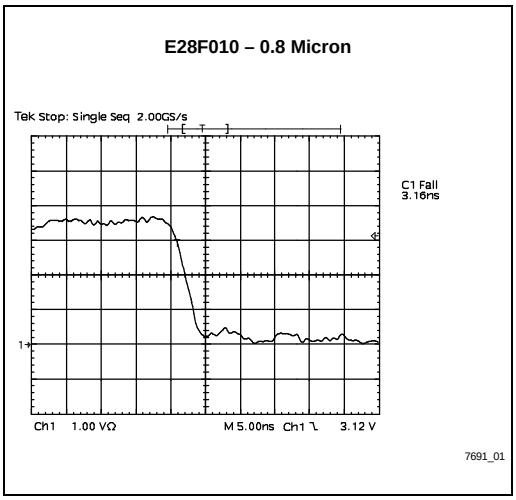

Figure 2. Newer Process 0.8 Micron Intel Flash Memory Devices Have Fast Output Slew Rates, 3.16 ns, in This Case

2.0 READ AND VERIFY PROBLEM IN SYSTEM APPLICATIONS

System applications not designed adequately for power and GND noise reduction may experience read and verify problems. These problems are enhanced by:

- Fast flash memory output slew rates
- All outputs switching to the same level simultaneously

To resolve random read and verify problems the root-causes must be clearly understood.

2.1 Root-Causes of Random Read and Verify Errors

The following root-causes of random read and verify errors can occur in both PROM programmer and embedded system applications. Some root-causes may be more prevalent in one environment over the other.

- High inductance of V_{CC} and GND printed circuit board traces
- Slow response time of the system power supply
- Increased V_{CC} and GND inductance due to the use of component sockets
- High V_{CC} inductance due to the use of a single V_{CC} pin on the flash memory component
- Resistance and inductance properties of flash memory package pins
- System board design – Are V_{CC} and GND planes used?

When one or more of the above factors are introduced in the system environment, false read and verify errors can occur. The errors are caused by spurious V_{CC} and GND noise transitions. In one user application, a GND noise transition of 3.44V Peak-Peak caused false read and verify errors (see Figure 3). This case is extreme but it shows the severity of noise transitions which cause read and verify errors. 1995 Intel Flash Memory databook specifications state that device operation is unpredictable if V_{CC} and GND are not maintained within the tolerance of V_{CC} ±10% and GND = 0V.

V_{CC} and GND noise transitions occur most frequently when all flash memory outputs switch simultaneously to the same level. In the event that all outputs switch from a low level to a high level, the instantaneous demand for current, di/dt, from the system power supply causes V_{CC} droop. The power supply cannot react quickly enough to the high demand for current, therefore V_{CC} droop occurs. When all outputs switch from a high level to a low level simultaneously, a surge of current is returned to the circuit. The power supply cannot compensate quickly enough to such a high amount of current being returned to the circuit, and a V_{CC} spike occurs. These V_{CC} spikes and droops are the root-cause of random read and verify errors.

To reduce the amplitude of V_{CC} noise transitions to an acceptable tolerance, V_{CC} ±10%, the instantaneous demand or instantaneous surge of current from the system power supply must be overcome.

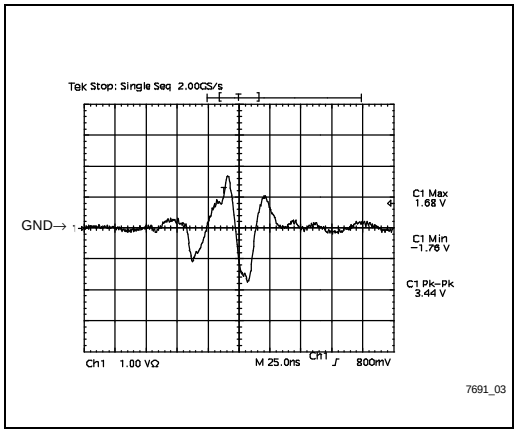

Figure 3. GND Noise Transition Measured at Flash Memory GND Pin

Example: False Program Verify Error in a PROM Programmer Environment

Let's investigate a program verify example to highlight the problem. As the flash memory cycles through address locations comparing data, a power transition of 3.44V P-P occurs. Suddenly, the flash V_{CC} and GND reference levels are increased ~1.68V or more while inputs to the flash memory remain at V_{IL} and V_{IH} levels. This causes the flash memory to internally change address locations. When program verify continues the buffer memory expects certain data for a particular address but since the flash memory has internally changed address locations it provides different data, resulting in a program verify miscompare. This sequence of events occurs at random address locations each time program verify is performed.

The program verify problem is not unique to any particular flash product but is an example of the type of issues system manufacturers may deal with on existing flash products.

3.0 HARDWARE OPTIMIZATIONS TO SYSTEM BOARDS AND COMPONENT INTERFACES

This section suggests hardware improvements design engineers may incorporate in their system designs to eliminate random read and verify errors. Not all suggested optimizations may be necessary to correct noise problems. The design engineer must review the electrical characteristics of each circuit and incorporate the optimization(s) best-suited for the particular environment.

Design engineers can reduce susceptibility to power induced noise problems by adhering to simple high-speed printed circuit board design guidelines. The following suggestions, if implemented in a PCB design, will reduce susceptibility to V_{CC} and GND noise-induced problems when programming high-speed flash memory components.

3.1 Hardware Design Optimizations to Reduce Noise Susceptibility

3.1.1 EMBEDDED SYSTEMS AND PROM PROGRAMMERS

- Keep V_{CC} and GND inductance to a minimum. Direct connections from the component socket to V_{CC} and GND planes on the system board will reduce inductance.
- Locate the power supply as close to the flash device as possible. This will minimize the inductance of V_{CC} and GND printed circuit board traces.
- Place 0.1 µF ceramic bypass capacitors as close to the flash component V_{CC} and GND, V_{PP} and GND pin(s) as possible. This will help suppress high frequency power transitions. Place a 4.7 µF electrolytic bypass capacitor as close to one V_{CC} and GND pin as possible. This will help suppress low-frequency power transitions.
- Keep power supply interconnections to a minimum. Interconnections can add inductance and capacitance to a circuit and will decrease and distort the circuit's ability to operate at high frequencies.
- Minimize susceptibility to signal crosstalk. Crosstalk, the electrical influence of one signal on another, alters the high frequency operating characteristics in a circuit. To reduce signal crosstalk avoid locating flash memory control signal printed circuit board traces in close proximity to power supply traces.

3.1.2 PROM PROGRAMMERS ONLY

- Slow down the slew rate of flash memory outputs. One method of slowing down slew rates is to include 50Ω or greater series resistors in the circuit for all outputs, (see Figure 4). By including series resistors the output slew rates will slow down enough to distribute the demand or surge of current, di/dt, over a longer time period, thus reducing the amplitude of power transitions.

CAUTION

If the random read and verify problem exists in an embedded system, be aware that adding series resistors to the data outputs will not only slow down the output slew rates, but will also slow down T_{ACC} times. In some applications, slower T_{ACC} could cause other timing problems.

- Component interfaces significantly affect the amplitude of V_{CC} and GND noise transitions by adding inductance to the circuit. Component sockets add inductance which increases the amplitude of noise transitions on V_{CC} and GND pins thus increasing susceptibility to read and verify problems. If a component socket must be used, then appropriate socket design considerations must be incorporated to reduce susceptibility to V_{CC} and GND noise-related problems.

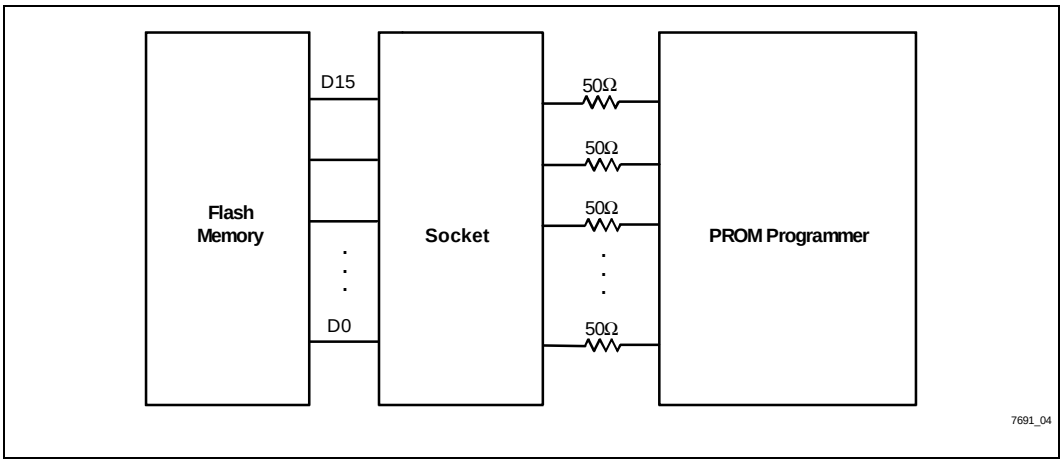

Figure 4. Series Resistors are Added to All Flash Memory Data Outputs to Slow the Output Slew Rates, Thus Reducing the Amplitude of Power and GND Noise Transitions

4.0 SOFTWARE OPTIMIZATIONS TO PROGRAMMING ALGORITHMS

This section outlines software optimizations that reduce device failures due to false read and verify errors. These optimizations are focused on modifications to algorithms for individual products.

Software Optimization 1: Precharge Data Bus via the CPU or PROM Programmer Drivers before Reading the Device

To reduce the amplitude of V_{CC} and GND noise transitions, try precharging the data bus with expected data before reading the flash memory (see Figure 5). By precharging the data bus, we use the slower slew rate pin drivers of the system CPU or PROM programmer to drive the data bus to expected levels. The slower slew rate drivers spread out the demand for current over a longer period of time reducing the amplitude of V_{CC} and GND noise transitions. Now, when the flash memory drives the data bus, the output levels are already at expected levels and high current draw does not occur.

Software Optimization 2: Toggle OE# at Each Address Location

Toggling OE# at each address location is another software optimization used to reduce the amplitude of V_{CC} or GND noise transitions. This suggestion applies to Intel Flash memory components that use both CE# and OE# control pins. If your programming algorithms switch CE# with each address location you may consider keeping CE# low while programming the entire memory array and switching OE# for each address location. CE# activates the flash memory control logic, input buffers, decoders and sense amplifiers. By activating all these device circuits at each memory location you are demanding more current from the power supply than is necessary. OE# gates the flash memory output through the data buffers during a read cycle. i.e., OE# activates less device circuitry than CE#. If CE# remains low and OE# is switched at each address location, less current draw from the power supply occurs and results in reduced amplitude of V_{CC} or GND transitions.

If this software optimization is implemented be certain to adhere to databook specifications that typically restrict input rise and fall times to < 10 ns, (10%–90%).

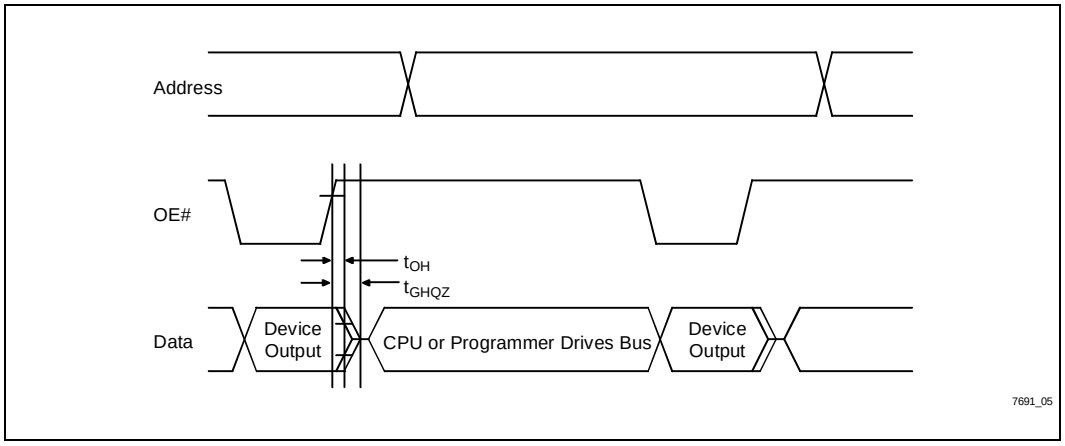

Figure 5. An Example of Precharging the Flash Memory Data Bus via the System CPU or PROM Programmer Pin Drivers

Software Optimization 3: Multiple Reads of a Failing Address Location in a PROM Programmer

Multiple reads of a failing address location does not reduce the amplitude of V_{CC} or GND noise transitions, it does provide a method to work around false program verify problems. When performing program verify and false errors occur try reading the same address location multiple times before failing the device. For example, if the failing address fails five consecutive program verify attempts then the device can be declared a failure due to program verify miscompare. If you are experiencing false program verify miscompares due to V_{CC} or GND noise transitions then the second or third attempt of reading the same address location should provide a successful program verify compare.

5.0 TEST PROCEDURE TO FIND PEAK POWER AND GND NOISE TRANSITIONS

To capture V_{CC} or GND noise transitions accurately, the test engineer must use appropriate test equipment. High bandwidth Digital Storage Signal Analyzers with fast sample rates will capture short duration noise transitions that cause random read and verify errors. The following equipment suggestions, if utilized, will insure you have the capability to capture V_{CC} or GND noise transitions:

Suggested Test Equipment Hardware Specifications to Capture High Frequency Noise Transitions

To capture high frequency noise transitions on flash memory V_{CC} or GND pins, your test equipment should perform to the following specifications:

- Digital Storage Signal Analyzer - 500 MHz or greater bandwidth
- Digital Storage Signal Analyzer - 2 Gigasample per second or faster digitizing rate
- F.E.T. probes - 500 MHz bandwidth or greater, CL < 2.0 pF, input resistance > 1 MΩ

Be certain to follow the Digital Signal Analyzer manufacturer's recommended warm-up procedure before you capture high frequency noise transitions. Equipment that has not thermally stabilized may yield inaccurate results. Probe compensation is also crucial to accurately capturing high frequency signals. After the recommended warm-up period the probes must be compensated per the manufacturer's instructions.

V_{CC} or GND high frequency transition measurements must be made as close as possible to the flash memory device pins for maximum accuracy. If possible, place the probe tip directly on the flash memory V_{CC} or GND pin. Probe GND leads must always be used and should be short in length to reduce GND loop potential. The

inductance of long GND leads can adversely affect the accuracy of high frequency measurements. An example of a short GND lead is a bayonet GND assembly. Bayonet GND assemblies limit GND leads to ~8 mm by connecting GND to the probe GND casing of the probe tip. This is most desirable. If it is physically impossible to use a short bayonet GND lead, increase the length of the GND lead to the shortest length necessary to connect the probe to GND.

Digital Storage Signal Analyzer Setup to Capture V_{CC} or GND Noise Transitions

The Signal Analyzer acquisition mode is crucial to displaying the captured signal. V_{CC} or GND noise transitions are quick infrequent events and must be captured and stored by the Digital Storage Signal Analyzer for analysis. The signal analyzer must be configured to single acquisition mode. Single acquisition mode will capture the selected signal when all trigger conditions have been satisfied and display the signal on the CRT indefinitely or until a new trigger condition is met. By using single acquisition mode the test engineer will have time to analyze signal characteristics of the captured signal.

Horizontal timebase, vertical amplitude, and vertical offset settings must be properly adjusted to allow the entire noise spike to appear on the CRT. The horizontal timebase can be set to ~20 ns/div so short time duration spikes will be visible. The vertical amplitude can be set to 1V/div to display signal aberrations. Adjust the vertical offset so the displayed signal will be centered on the CRT for clear viewing.

Trigger level is important in capturing peak V_{CC} or GND transitions. Begin measurements by setting the trigger level to a value known to cause a trigger event, i.e., +5.0V for V_{CC} measurements. To find the maximum peak transition move the trigger level up to +5.25V. If the signal analyzer triggers at +5.25V then increase the trigger level again incrementally. Keep increasing the trigger level until the signal analyzer no longer triggers.

Now decrease the trigger level in smaller increments until you find a trigger point. This is the maximum peak transition you have been seeking. To capture the minimum peak transition perform the same trigger level search but decrease trigger levels each time, i.e., begin the search at +5.0V, then incrementally decrease to +4.75V, +4.5V, etc. When the signal analyzer no longer triggers increase the trigger level in smaller increments until you find a trigger point. This is the minimum peak transition you have been seeking.

6.0 CONCLUSION

The read and verify problem discussed in this technical brief can occur in PROM programmer environments and in embedded system applications. The problem is a function of the flash memory requiring much current, di/dt, in a short timeframe and the system power supply not being able to support the flash memory current requirements as quickly as needed.

The suggestions provided in this document, if implemented as outlined, will either reduce or eliminate false random read and verify problems from a PROM programmer or embedded system environment. Each circuit is unique and should be evaluated by a design engineer prior to implementing any suggestions from this technical paper.

7.0 ADDITIONAL INFORMATION

7.1 References

Order Number	Document
218830	1995 Flash Memory Databook, Volume 1

7.2 Revision History

Number	Description
-001	Original Version

Filename:	297691_1.DOC
Directory:	C:\TESTDOCS\ORIGDOCS
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